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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/568,620	02/16/2006	Hideo Taniuchi	289515467	2879

53067 7590 05/15/2008

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EXAMINER	
KHOSRAVIANI, ARMAN	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
05/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/568,620	TANIUCHI, HIDEO	
	Examiner	Art Unit	
	ARMAN KHOSRAVIANI	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) *4-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/16/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. This application contains claims directed to more than one species of the generic invention. These species are deemed to lack unity of invention because they are not so linked as to form a single general inventive concept under PCT Rule 13.1.

The species are as follows:

I. Figure 1 II. Figure 2 III. Figures 3-5

Applicant is required, in reply to this action, to elect a single species to which the claims shall be restricted if no generic claim is finally held to be allowable. The reply must also identify the claims readable on the elected species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered non-responsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

The claims are deemed to correspond to the species listed above in the following manner:

Claims 1-3 correspond to Figure 1, Species I

Claims 4-6 correspond to Figure 2, Species II

Species III is not claimed

The following claim(s) are generic: 1.

The species listed above do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, the species lack the same or corresponding special technical features for the following reasons: Applicant's invention disclosed in Figures 1 and 2 lack a special technical feature over the prior art shown in Figure 6.

The expression "special technical features" shall mean those technical features that define a contribution which each of the claimed inventions, considered as a whole, makes over the prior art. *PCT Rule 13.2*

Figure 6 discloses the particulars of Applicant's invention with the exception of a voltage conversion circuit and interconnects between the first and second semiconductor chip contained in Figures 1 and 2. These two features for forming integrated circuits and controlling their voltage are well known and by no means special technical features in the art. Thus special technical feature is not present, since the group of features in the prior art, Figure 6, is common to Figures 1 and 2, and the addition of a voltage conversion circuit and interconnects between first and second semiconductor chips does promulgate unity of invention as applicant's contribution resides in bulk on the features of the disclosed prior art Figure 6.

2. During a telephone conversation with Atty. Roger Parkhurst on May 7, 2008 a provisional election was made with traverse to prosecute the invention of I, claims 1-3. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 4-6 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: ***(See MPEP Ch. 2141)***
>
> a. Determining the scope and contents of the prior art;
> b. Ascertaining the differences between the prior art and the claims in issue;
> c. Resolving the level of ordinary skill in the pertinent art; and
> d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's cited prior art of figure 6 in view of Heberle et al. (WO/2003/065453).

Regarding claim 1, Applicant's cited prior art teaches (fig. 6) a multi-chip-type semiconductor device comprising a first semiconductor chip 1 and a second semiconductor chip 2 in a package 3, wherein said first semiconductor chip comprises a first serial decoder 6, external connection terminals 12 led out of the package, and external connection portions 13 for connection to the external connection terminals, said

second semiconductor chip 2 comprises a second serial decoder 5, and serial data input through the external connection terminals 23 is transmitted to the second serial decoder 5 via the voltage conversion circuit 21. Applicant cited prior art fails to teach the first and second semiconductor chips being connected to each other in a package, a first semiconductor chip comprising a plurality of first inter-chip connection portions for connection to the second semiconductor chip, a second semiconductor chip comprising a plurality of second inter-chip connection portions for connection to the first semiconductor chip, bonding wires for directly connecting the plurality of first inter-chip connection portions and the plurality of second inter-chip connection portions to each other, and serial data input through the external connection terminals transmitted to the second serial decoder via the first and second inter-chip connection portions in addition to the voltage conversion circuit. Note, Applicant's cited prior art teaches (fig. 6) first and second serial decoders on first and second chips, respectively, but lacks an interconnection between the two chips and a voltage regulator on the first chip for transferring serial data input to a second serial decoder (i.e. from first chip to second chip).

However, Heberle teach (fig. 5, where terminals are at the ends of bonding wires 3 within package 2) the first 8 and second 9 semiconductor chips being connected to each other in a package 2, a first semiconductor chip comprising a plurality of first inter-chip connection portions 3 for connection to the second semiconductor chip, a second semiconductor chip comprising a plurality of second inter-chip connection portions 3 for connection to the first semiconductor chip, bonding wires for directly connecting the

plurality of first inter-chip connection portions and the plurality of second inter-chip connection portions to each other (inter-chip connection portions are formed at the ends of bond wires). Heberle further teaches a serial data input (from wires 3 as an input to functional circuit 7) through the external connection terminals (ends of the terminals 3) and further teaches the voltage conversion circuit (subcircuits of 7 which includes general function circuit 8, page 2, "Regelschaltungen fur Versorgungsspannungen" supply voltage regulator). Applicant's cited prior art (fig. 6) teaches the first and second serial decoders, but lacks an interconnection and a voltage regulator on a first chip, Heberle teaches a voltage regulator on chip 8 and interconnects between the two chips 8 and 9 for transferring serial data input to a second chip 9.

Since both Heberle and Applicant's cited prior art figure 6 teach the multi-chip-device above, it would have been obvious to have the first and second semiconductor chips being connected to each other in a package, a first semiconductor chip comprising a plurality of first inter-chip connection portions for connection to the second semiconductor chip, a second semiconductor chip comprising a plurality of second inter-chip connection portions for connection to the first semiconductor chip, bonding wires for directly connecting the plurality of first inter-chip connection portions and the plurality of second inter-chip connection portions to each other, and serial data input through the external connection terminals transmitted to the second serial decoder via the first and second inter-chip connection portions in addition to the voltage conversion circuit of Heberle in Applicant's cited prior art figure 6 for the benefit of reducing overall size of a

multi-chip-type semiconductor device by eliminating the need for an external voltage conversion circuit.

Regarding claim 2, Applicant's cited prior art teaches (fig. 6, par.9) a high voltage can be applied to the first semiconductor chip 1, and the second semiconductor chip 2 has a withstand voltage lower than that of the first semiconductor chip and lower than the voltage of the serial data externally applied (through voltage regulator circuit 21, see par.7).

Regarding claim 3, Applicant's cited prior art teaches (fig. 6, par.8) the first semiconductor chip and the second semiconductor chip controlled by serial data from a microcomputer 8.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ARMAN KHOSRAVIANI whose telephone number is (571)272-2554. The examiner can normally be reached on Monday to Friday, 7:30a - 5:00p (Eastern Time).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AK

/Steven Loke/
Supervisory Patent Examiner, Art Unit 2818